DSP UNIT FOR MULTI-LEVEL GLOBAL ACCUMULATION

ABSTRACT OF THE DISCLOSURE

[0097] In one embodiment, a digital signal processor (DSP) is described for multi-level global accumulation. The DSP includes a plurality of absolute difference determinators in a first stage. The absolute difference determinators may include arithmetic logic units (ALUs) in combination with multiplexers. By using multiple absolute difference determinators, the throughput of the DSP is increased. An existing multiplier may be reconfigured into an adder tree to process the absolute difference results obtained in the first stage. To further increase throughput, multiple DSPs with multiple absolute difference determinators may be operated in parallel.